Profile of Dr. A.V.Ananthalakshmi

1. Present Position: Assistant Professor
Dept. of Electronics and Communication Engg.
Pondicherry Engineering College,
Pondicherry – 605 014.
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Mobile : 6379670893
Phone : 0413-2655281-666

2. Date of Birth: 11.04.1980

3. Academic Details:

University	Degree	Year of passing	Class	Specialization
Madras University	**B.E**	2001	First class with Distinction	Electronics and Communication
Manipal University	**M.S**	2003	First class with Distinction	VLSI - CAD
Pondicherry University	**Ph.D**	2015	Commended	Low Power VLSI Design

3. Employment record: **13 years experience**

University/college	Designation	Period
Velammal Engineering College	Lecturer	June 2003 – May 2004
R.M.K. Engineering College	Lecturer	July 2004 – Dec 2006
IFET Engineering College	Lecturer	Jan 2006 – 9th August 2007
Pondicherry Engineering College	Assistant Professor	10th August 2007 – till date

4. Publications:

Conferences:

1. G.F.Sudha, **A.V.AnanthaLakshmi** and B.Sarojini, "Energy Efficient Architecture for Portable Device", Proceedings of the International Conference on Frontiers of Computer Science, August 2011, pp. 91 – 93. ISBN No.: 978-81-921929-0-1

2. **A.V.AnanthaLakshmi**, G.F.Sudha, "Design of a Novel Reversible Full adder and Reversible Full Subtractor", **Springer** Proceedings of the International Conference on Advances in Computing and Information Technology(ACITY), July 2012, Vol. 178, pp.623 – 632. ISBN No.: 978-3-642-31599-2
3. **A.V.AnanthaLakshmi**, G.F.Sudha, "An Efficient Implementation of a Reversible Single Precision Floating Point Multiplier Using 4:3 Compressor", **Elsevier** Proceedings of the International Conference on Advances in Information Technology and Mobile Communications(AIM), April 2013, pp. 229 – 238.
4. **A.V.AnanthaLakshmi**, G.F.Sudha, "Transistor Representation of a Low Power Reversible 32-bit Comparator", **Springer** Proceedings of the International Conference on Advanced Computing, Networking and Informatics (ICACNI), June 2013, Vol. 243, pp. 63 -74, ISSN : 1867-5662
5. S.S. Gayathri, **A.V.AnanthaLakshmi**, "Design and implementation of efficient reversible even parity checker and generator", **IEEE Proceedings** of the International Conference on Science Engineering and Management Research (ICSEMR), Nov. 2014, pp. 1 – 4.
6. Ruth Joanna, **A.V.AnanthaLakshmi**," Design and Implementation of efficient adaptive FIR filter based on Distributed Arithmetic", **IEEE Proceedings** of the International Conference on Innovations in Information, Embedded and Communication Systems (ICIECS), Apr. 2015, pp. 164 – 167.
7. A. Anjana and A. V. Ananthalakshmi, "Design Of Reversible 32-Bit BCD Add-Subtract Unit Using Parallel Pipelined Method", **IEEE Proceedings** of the 2nd International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), February 2016, pp. 162 – 165.

Journals:

1. **A.V.AnanthaLakshmi**, G.F.Sudha, "Design of a reversible single precision floating point subtractor", **SpringerPlus Journal, (SCIE Indexed), Article Metrics : 2685,** 3 : 11, ISSN: 2193-1801, January 2014, doi:10.1186/2193-1801-3-11.
2. **A.V.AnanthaLakshmi,** G.F.Sudha, " Area and Speed Efficient Reversible Fused Radix-2 FFT Unit Using 4:3 Compressor", **International Journal on Recent Trends in Engineering and Technology**, pp. 172 – 186, vol. 10, no.2, ISSN: 2158-5563, January 2014, doi: 01.IJRTET.10.2.1453.
3. **A.V.AnanthaLakshmi,** G.F.Sudha, " Design of 4-Bit Reversible Shift Registers", **WSEAS Transactions on Circuits and Systems, (Scopus Indexed),** pp. 376 – 385, vol. 12, no.12, Print ISSN: 1109-2734, E-ISSN : 2224 – 266X, December 2013,.
4. **A.V.AnanthaLakshmi**, G.F.Sudha, "Design of an efficient reversible single precision floating point adder", **International Journal of Computational**

Intellgent Studies , (ACM Digital Library Indexed), pp. 2 – 30, vol. 4, no. 1, ISSN online: 1755-4985, ISSN print: 1755-4977, June 2015, doi: 10.1504/IJCISTUDIES.2015.069830.

5. **A.V.AnanthaLakshmi** and G.F.Sudha, "Design of a Reversible Fused Radix- 2 Floating Point FFT Unit using 3:2 Compressor," ***International Journal of New Computer Architectures and Applications***, ***Society of Digital Information and Wireless Communications***, pp. 201 – 210, vol. 4, no. 4, E-ISSN: 2220-9085, December 2014, doi: http://dx.doi.org/10.17781/p0020.
6. **A.V.AnanthaLakshmi** and G.F.Sudha, "Design of an Efficient Reversible Single Precision Floating Point Multiplier," ***Journal of Bioinformatics and Intelligent Control***, ***American Scientific Publisher***, pp. 21 – 30, vol. 4, no. 1, ISSN:1546-1998, March 2015.
7. **A. V. AnanthaLakshmi**, G. Harish, BokkaBindu Kumar, "VLSI Implementation of Efficient Lossless Fuzzy Based ECG Encoder," ***Journal of Bioinformatics and Intelligent Control***, ***American Scientific Publisher***, pp. 10 – 15, vol. 4, no. 1, ISSN:1546-1998, March 2015.
8. P. Rajagopalan and **A.V. Ananthalakshmi**, "VLSI Implementation of Reverse Converter via Parallel Prefix Adder for Signed Integers", ***International Journal of Computer Science and Information Security***, pp.8-12, vol.14, CIC 2016, October 2016.
9. **A.V.Ananthalakshmi**, "Effective Diagnosis of Diabetes Mellitus Using Neural Networks and its Hardware Implementation on FPGA", ***International Journal of Computer Science and Information Security,*** pp.8-12, vol.15, no.1, February 2017.
10. **A.V. Ananthalakshmi** and G.F.Sudha, "A novel power efficient 0.64-GFlops fused 32-bit reversible floating point arithmetic unit architecture for digital signal processing applications", ***Microprocessors and Microsystems, Embedded Hardware Design, Elsevier***, pp. 366 – 385, vol. 51, June 2017, ISSN - 0141-9331.
11. **A.V. Ananthalakshmi** and G.F.Sudha, "Design of a reversible floating point square root using modified non-restoring algorithm", ***Microprocessors and Microsystems, Embedded Hardware Design, Elsevier***, pp. 39 – 53, vol. 50, May 2017.
12. K. Gomathy, **A.V.Ananthalakshmi**, "Design of a Secure VLIW Based Reconfigurable CRYPTO Processor Architecture", ***International Journal of Control Theory and Applications***, pp. 309-313, vol.10, no.36, 2017, ISSN : 0974-5572.
13. **A.V.Ananthalakshmi**, P. Rajagopalan, "VLSI implementation of residue number system based efficient digital signal processor architecture for wireless sensor nodes", ***International Journal of Information Technology, Springer,*** 1-12, Mar 2019, DOI : 10.1007/s41870-019-00297-8, ISSN:

5. Externally Funded Projects:

Funding Agency: UGC Minor Research Project

Title: VLSI Implementation of Speed and Power Efficient Digital Signal Processor Architecture for Wireless Sensor Nodes

Financial Outlay: Rs. 3,95,820/-

Duration: 2017-2019 (Two years)

6. Co-ordinated FDP/Seminar/Workshop:

1. One week FDP on "Interactive System Design Using Labview" from 19th January to 23rd January 2015.
2. AICTE Sponsored one week QIP Short Term Course on "Emerging Trends in VLSI for Communication" from 2nd March to 6th March, 2015.
3. One day workshop on "VLSI Design usingVirtual Lab" on 15th March 2015.
4. Two Days Hands-on Training Programme on "TMS320C6745 Digital Signal Processor" in Collaboration with Pantech Solutions, Chennai from 28th to 29th April 2015.
5. Three Days on Hands on Workshop on "Hard and Soft Core Processor based Embedded System Design" from 13th December to 15th December 2017.
6. Two Days Hands-on Workshop on "Robotics" from 24th February to 25th February 2017.

7.Membership of Professional Organization: Life member of ISTE

8. Research Guidance:

Reviewer

	Name of the Journal	**Publisher**
i.	International Journal of Theoretical Physics	Springer
ii.	International Journal of Biomedical Engineering & Technology	Inderscience
iii.	International Journal of Autonomic Computing	Inderscience
iv.	International Journal of Sensors, Wireless Communication and Control	Bentham Science
v.	IEEE Transactions on VLSI Systems	IEEE
vi.	Circuits, Systems and Signal processing	Springer

9. Conferences, short term courses etc participated: 24

Course Title	**Sponsored By**	**Conducting Institute**	**Date From**	**Date To**
Design of High Performance Systems Using FPGAs	ISTE	NIT, Trichy	January 25, 2009	January 29, 2009
Mission 10X	ISTE	PEC	February 16, 2009	February 20, 2009

Recent Trends in Cloud Security	DIT	Dept of CSE, PEC	March 26, 2012	March 30, 2012
Design of Embedded Systems - Issues and Challenges	AICTE	Dept. of CSE, PEC	April 16, 2012	April 27, 2012
Fuzzy Techniques in Image Processing	AICTE	Dept. of ECE, Mailam Engineering College	May 21, 2012	May 25, 2012
Emphasis on Smart Operation and Control of Power Markets Using Power Electronic Components	TEQIP	Dept. of EEE, PEC	November 19, 2012	November 23, 2012
Recent Advances in Green Engineering	TEQIP	Dept. of ECE, PEC	December 03, 2012	December 07, 2012
Security in Wireless Heterogenous Networks	AICTE	Dept. of ECE, PEC	April 15, 2013	April 26, 2013
Wireless Sensor Networks Issues and Challenges	TEQIP	Dept. of ECE, PEC	November 11, 2013	November 15, 2013
Nano Engineering Materials	ISTE	Physics Dept, PEC	December 13, 2012	December 23, 2012
STC on Microelectronics for wireless communication	ISTE - SRM	Department of ECE, Pondicherry Engineering College	May 06, 2013	May 11, 2013
One week FDP on Interactive System Design using Labview	DIT, Puducherry	Department of ECE, Pondicherry Engineering College	January 19, 2015	January 23, 2015
One Day Workshop on Importance of Reforms in Higher Education	RUSA	Pondicherry Engineering College	August 31, 2015	August 31, 2015
Workshop on Programme Educational Objectives and Programme Outcomes	RUSA	Pondicherry Engineering College	August 20, 2015	August 20, 2015
FDP on VLSI Design using NI Hardware and Software	Puducherry e-Governance Society	Department of ECE, Pondicherry Engineering College	September 22, 2015	October 01, 2015
STTP on Recent Trends in Optimization Techniques and Applications	TEQIP	Department of CSE, Pondicherry Engineering College	January 04, 2016	January 09, 2016

STTP on Bio-Signal Processing for Telemedicine Applications	TEQIP II	Department of ECE, Pondicherry Engineering College	June 27, 2016	July 02, 2016
Symposim	e-Yantra	IIT Bombay	April 11, 2016	April 12, 2016
Interdisciplinary STC on ICT Solutions for Issues and Challenges in Smart Grid Technology	AICTE QIP	Department of EEE & Department of IT, Pondicherry Engineering College	November 28, 2016	December 02, 2016
STC on Enabling Technologies to aid Smart City Framework	AICTE QIP	Department of ECE & Department of CSE, Pondicherry Engineering College	February 06, 2017	February 10, 2017
5G mm Wave Radio Transmission for Ultra-High Speed Wireless Technologies	AICTE	Department of ECE, Pondicherry Engineering College	November 13, 2017	November 17, 2017
Nascent Generation and Distribution Technologies and Potential Research Problems in Power Systems	AICTE-QIP	Department of EEE, Pondicherry Engineering College	December 04, 2017	December 08, 2017
Application of Micro Grid in Distributed Generation Together with Clean Energy Technology	AICTE-QIP	Department of EEE, Pondicherry Engineering College	January 29, 2018	February 02, 2018

10. Field of Interest: Low Power VLSI Design, Reversible Logic Arithmetic Circuits.